

## CLAIMS

1 – 7. (cancelled)

8. (currently amended) A circuit comprising:

a source register with the plurality of bits divided into a plurality of first level subsets;  
means for identifying the bits in each subset which are transfer bits and non-transfer bits;  
arranger means for aligning the transfer data bits in each first level subset to a first side thereof to form corresponding second level subsets of the transfer data bits;  
a destination register; and

coupling means for loading the transfer data bits from the second level subsets into the destination register aligned to the first side of the destination register;

wherein the arranger means comprises a plurality of arrangers each for a receiving a set of mask bits, each set of mask bits corresponding to one of the arrangers, each arranger corresponding to a subset of the first level subsets, each arranger comprising:

a first multiplexer having a first input coupled to receive a first bit from the subset of the first level subsets to which the arranger corresponds, a second input coupled to receive a second bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving a first mask bit from the set of mask bits to which the arranger corresponds, and an output;

a second multiplexer having a first input to receive the first bit, a second input coupled to the output of the first multiplexer, a control input for receiving a second mask bit from the set of mask bits to which the arranger corresponds, and an output;

a third multiplexer having a first input coupled to the output of the first multiplexer, a second input coupled a third bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving the second mask bit, and an output;

a fourth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled a fourth bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving a third mask bit from the set of mask bits to which the arranger corresponds, and an output as a first output of the arranger;

a fifth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled to the output of the second multiplexer, a control input for receiving the third mask bit, and an output as a second output of the arranger; and

a sixth multiplexer having a first input coupled to the output of the second multiplexer, a second input coupled to receive the first bit, a control input for receiving the third mask bit, and an output as a third output of the arranger.

9. (original) The circuit of claim 8 further comprising a combiner means for combining pairs of the second level subsets, each pair comprising a first of the pair and a second of the pair, by shifting the transfer data bits of the first of the pairs to form shifted transfer bits and combining said shifted transfer bits with the second of the pairs.

10. (cancelled)

11. (original) The circuit of claim 9, wherein each combiner means comprises:

a first plurality of multiplexers coupled to the first of the pair and a first mask signal;

a second plurality of multiplexers coupled to the first plurality of multiplexers and a second mask signal; and

a third plurality of multiplexers coupled to the second plurality of multiplexers and a third mask signal.

12. (currently amended) A circuit, comprising:
  - a source register having a plurality of bits and for containing transfer and non-transfer data contained in first and second subsets of the plurality of bits;
  - a destination register;
  - a first arrangement means coupled to the first subset for placing the transfer bits contained in the first subset on a first side of the first arrangement means;
  - a second arrangement means coupled to the second subset for placing the transfer bits contained in the second subset on the first side of the first arrangement means;
  - shifter/combiner means for shifting the data in the second arrangement means toward the first side of the shifter/combiner means by an amount equal to the number of non-transfer bits in the first subset; and
  - coupling means for coupling the contents of the first and second means into the destination register;

wherein the first arrangement means comprises:

  - a first multiplexer having a first input coupled to receive a first bit from the first subset, a second input coupled to receive a second bit from the first subset, a control input for receiving a first mask bit, and an output;
  - a second multiplexer having a first input to receive the first bit, a second input coupled to the output of the first multiplexer, a control input for receiving a second mask bit, and an output;
  - a third multiplexer having a first input coupled to the output of the first multiplexer, a second input coupled a third bit from the first subset, a control input for receiving the second mask bit, and an output;
  - a fourth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled a fourth bit from the first subset, a control input for receiving a third mask, and an output as a first output of the first arrangement means;
  - a fifth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled to the output of the second multiplexer, a control input for receiving the third mask bit, and an output as a second output of the arrangement means; and

a sixth multiplexer having a first input coupled to the output of the second multiplexer, a second input coupled to receive the first bit, a control input for receiving the third mask bit, and an output as a third output of the arrangement means.

13. (original) The circuit of claim 12, wherein the coupling means is further characterized as coupling the contents of the first and second means into the first side of the destination register.

14. (cancelled)

15. (original) The circuit of claim 12, wherein the shifter/combiner means comprises:  
a first plurality of multiplexers coupled to the second arrangement means and a first mask signal;  
a second plurality of multiplexers coupled to the first plurality of multiplexers and a second mask signal; and  
a third plurality of multiplexers coupled to the second plurality of multiplexers and a third mask signal.